*Fig. 3A**(PRIOR ART)*

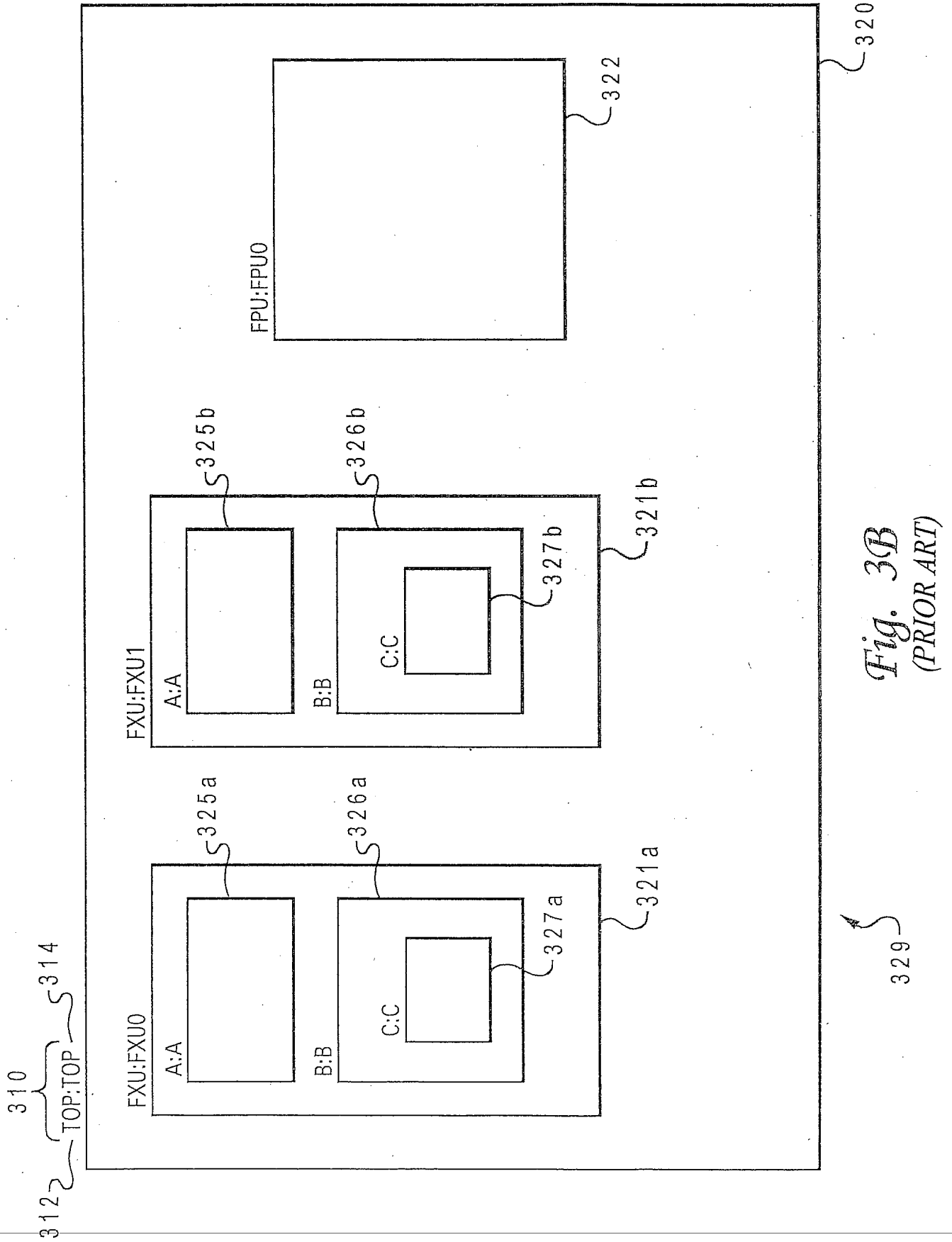


Fig. 3B
(PRIOR ART)

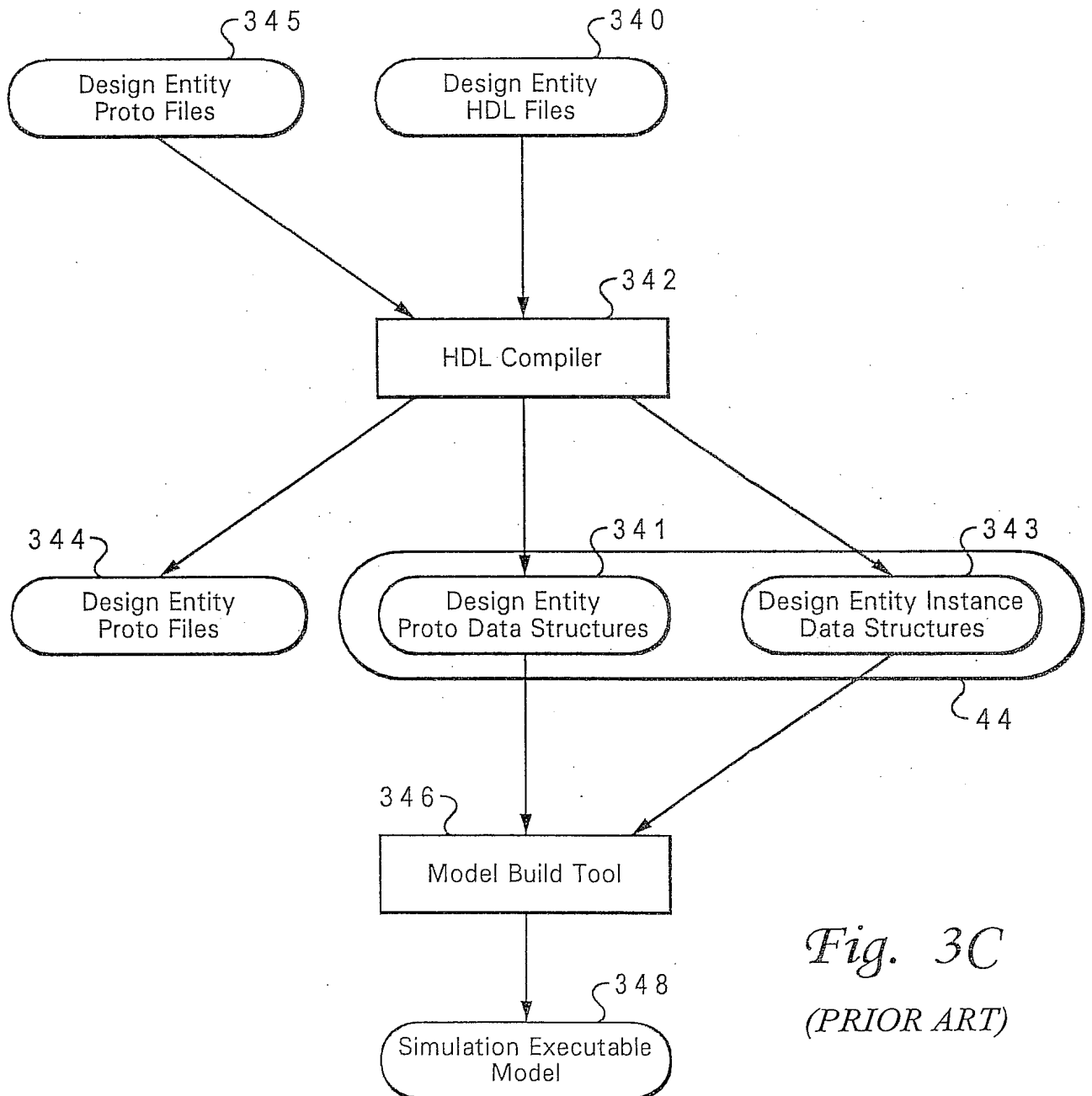
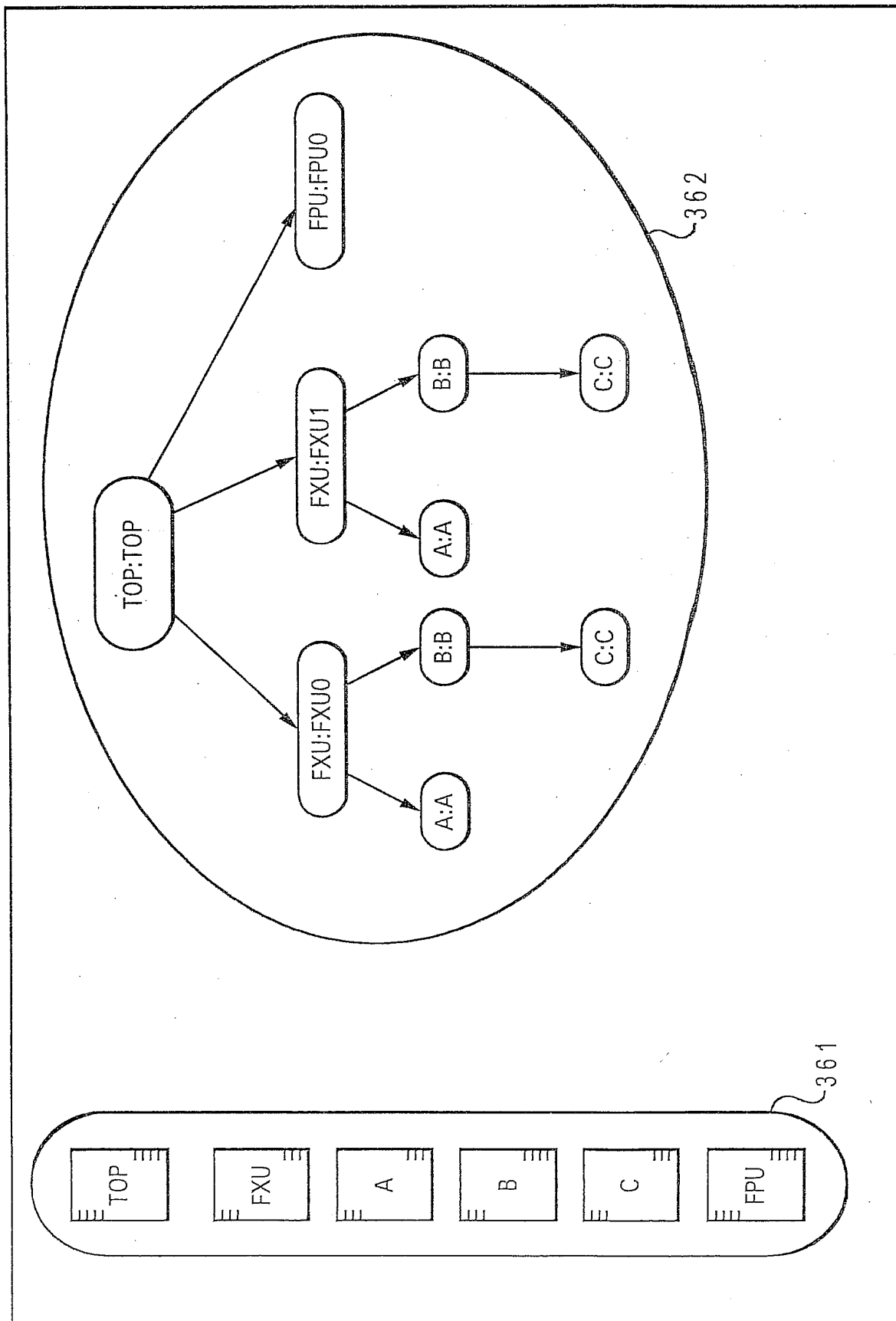


Fig. 3C
(PRIOR ART)



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Fig. 3D
(PRIOR ART)

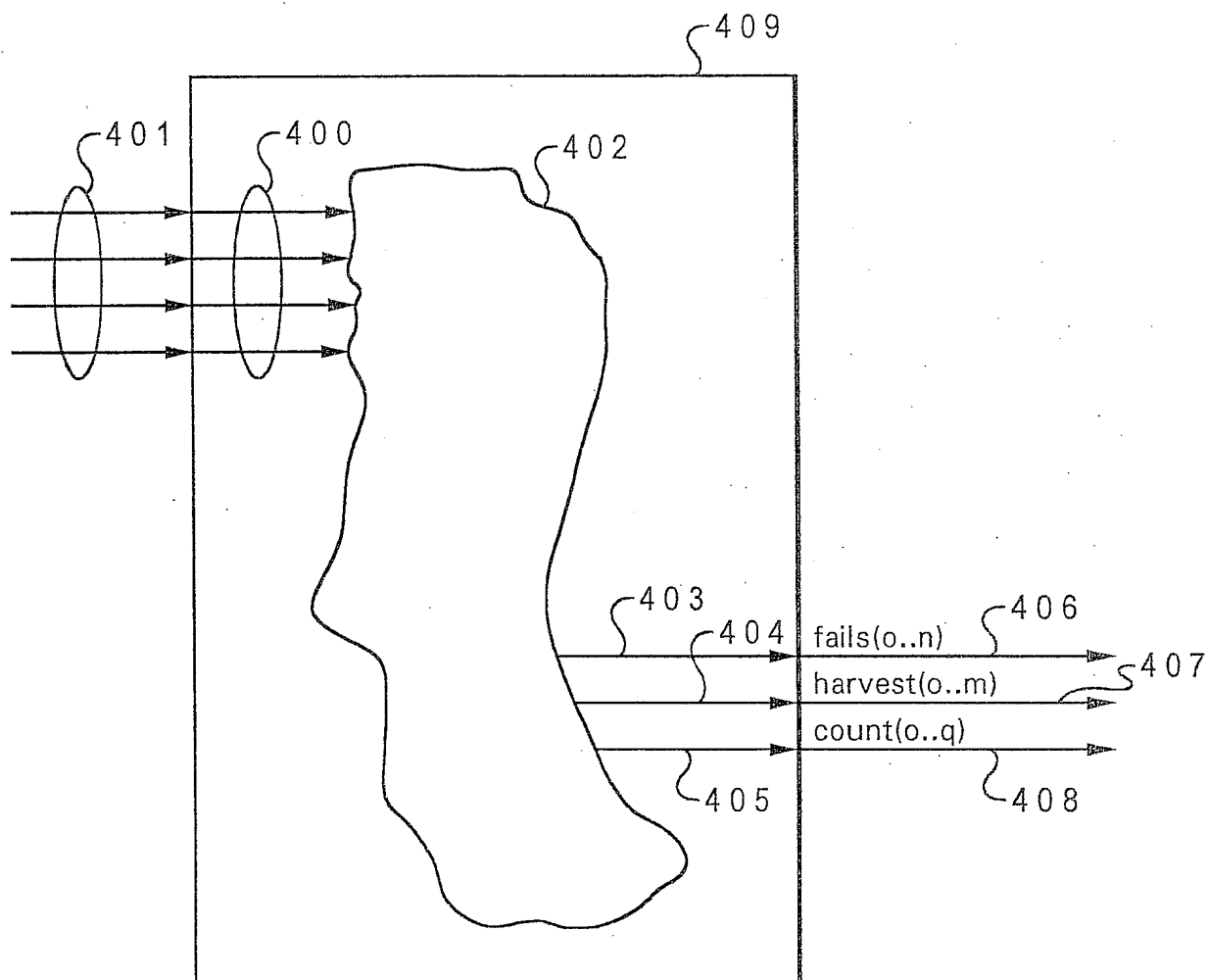


Fig. 4A
(PRIOR ART)

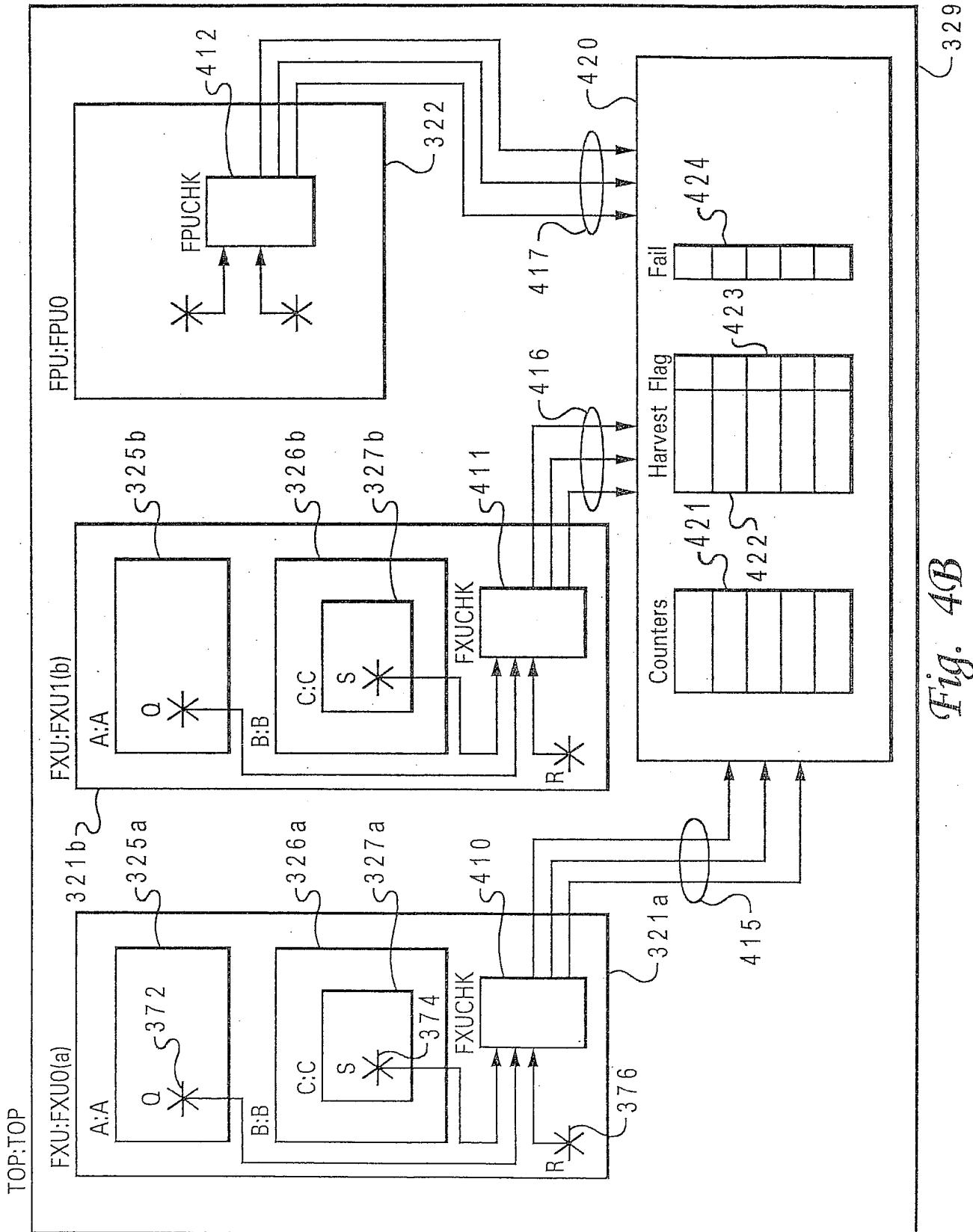


Fig. 4B
(PRIOR ART)

```

ENTITY FXUCHK IS
    PORT(
        S_IN      : IN std_ulogic;
        Q_IN      : IN std_ulogic;
        R_IN      : IN std_ulogic;
        clock      : IN std_ulogic;
        fails      : OUT std_ulogic_vector(0 to 1);
        counts     : OUT std_ulogic_vector(0 to 2);
        harvests   : OUT std_ulogic_vector(0 to 1);
    );
4 5 2 { --!! BEGIN
      --!! Design Entity: FXU;
4 5 3 { --!! Inputs
      --!! S_IN      => B.C.S;
      --!! Q_IN      => A.Q;
      --!! R_IN      => R;
      --!! CLOCK     => clock;
      --!! End Inputs
4 5 4 { --!! Fail Outputs;
      --!! 0 : "Fail message for failure event 0";
      --!! 1 : "Fail message for failure event 1";
      --!! End Fail Outputs;
4 5 5 { --!! Count Outputs;
      --!! 0 : <event0> clock;
      --!! 1 : <event1> clock;
      --!! 2 : <event2> clock;
      --!! End Count Outputs;
4 5 6 { --!! Harvest Outputs;
      --!! 0 : "Message for harvest event 0";
      --!! 1 : "Message for harvest event 1";
      --!! End Harvest Outputs;
4 5 7 { --!! End;

ARCHITECTURE example of FXUCHK IS
    BEGIN
        ... HDL code for entity body section ...
    END;

```

4 5 0

4 5 1

4 4 0

4 5 8

Fig. 4C
(PRIOR ART)

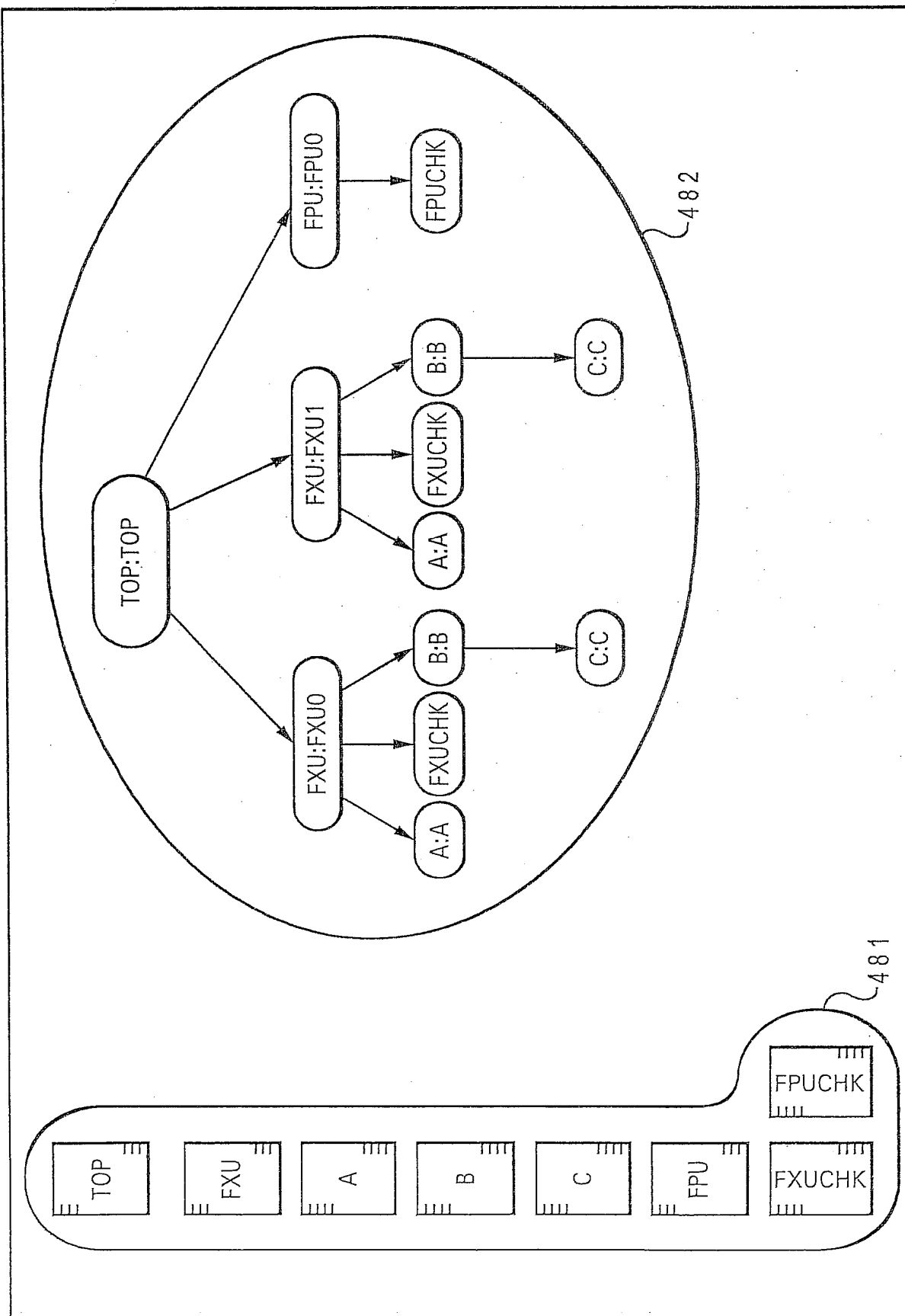


Fig. 4E
(PRIOR ART)



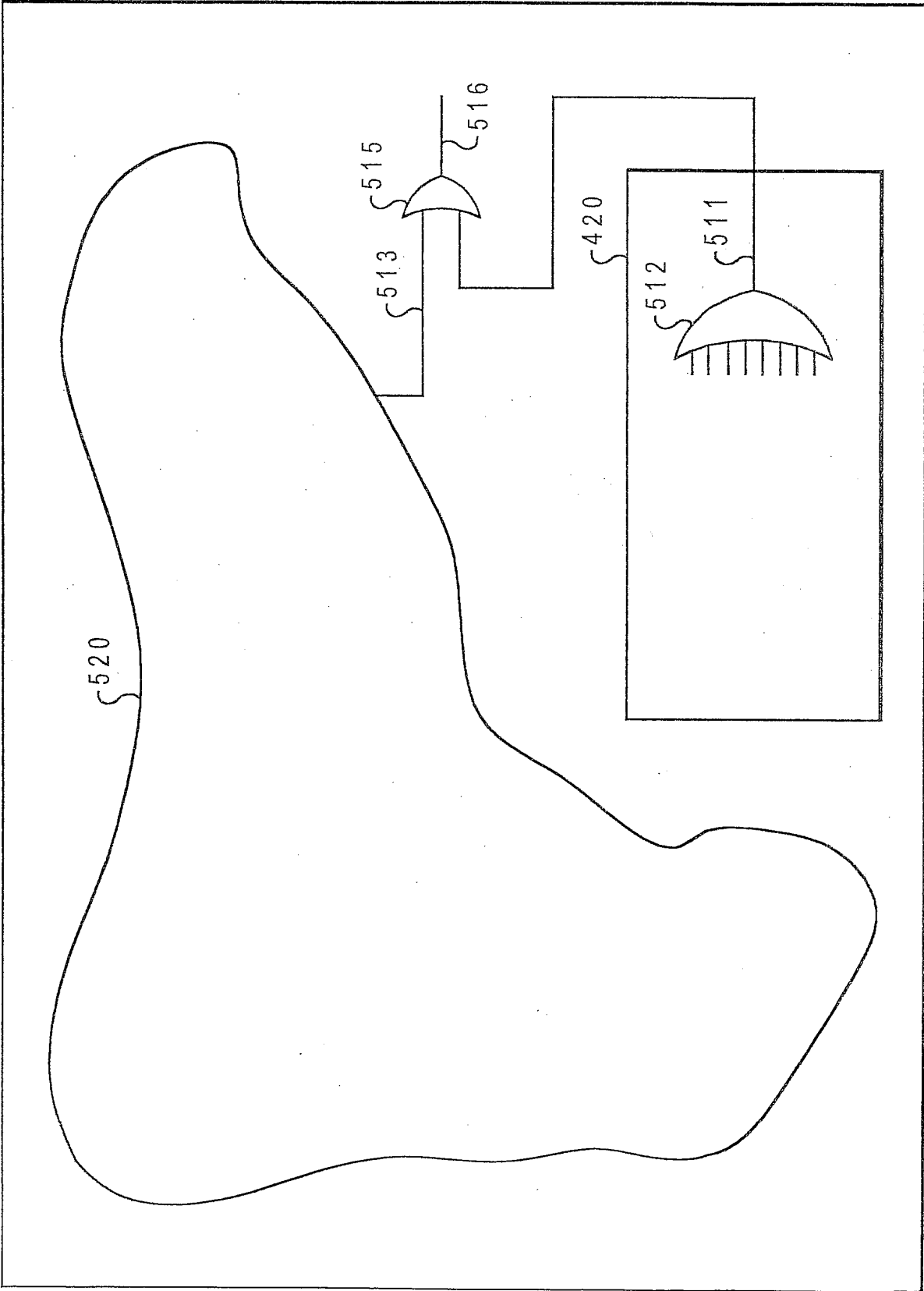


Fig. 5B
(PRIOR ART)

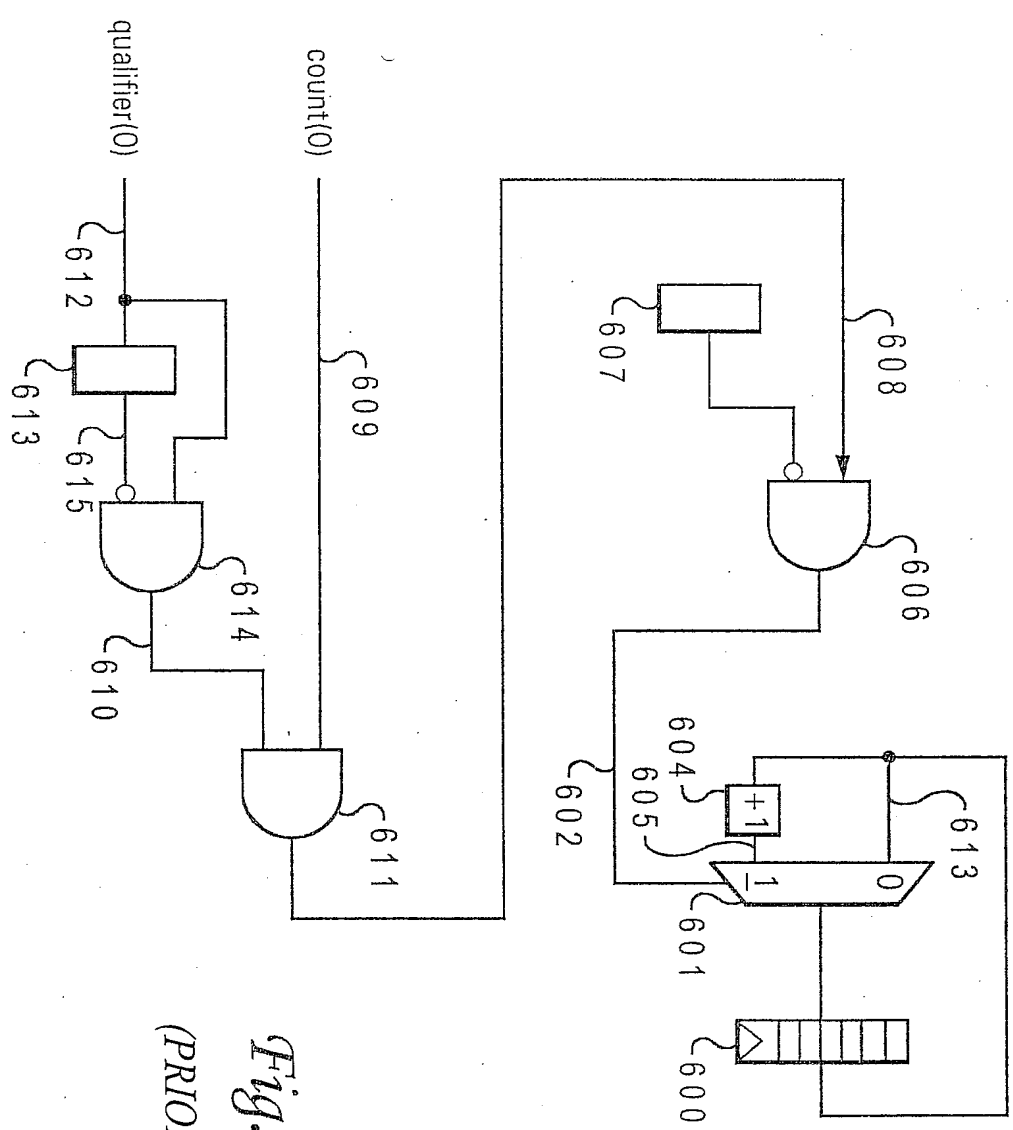


Fig. 6A
(PRIOR ART)

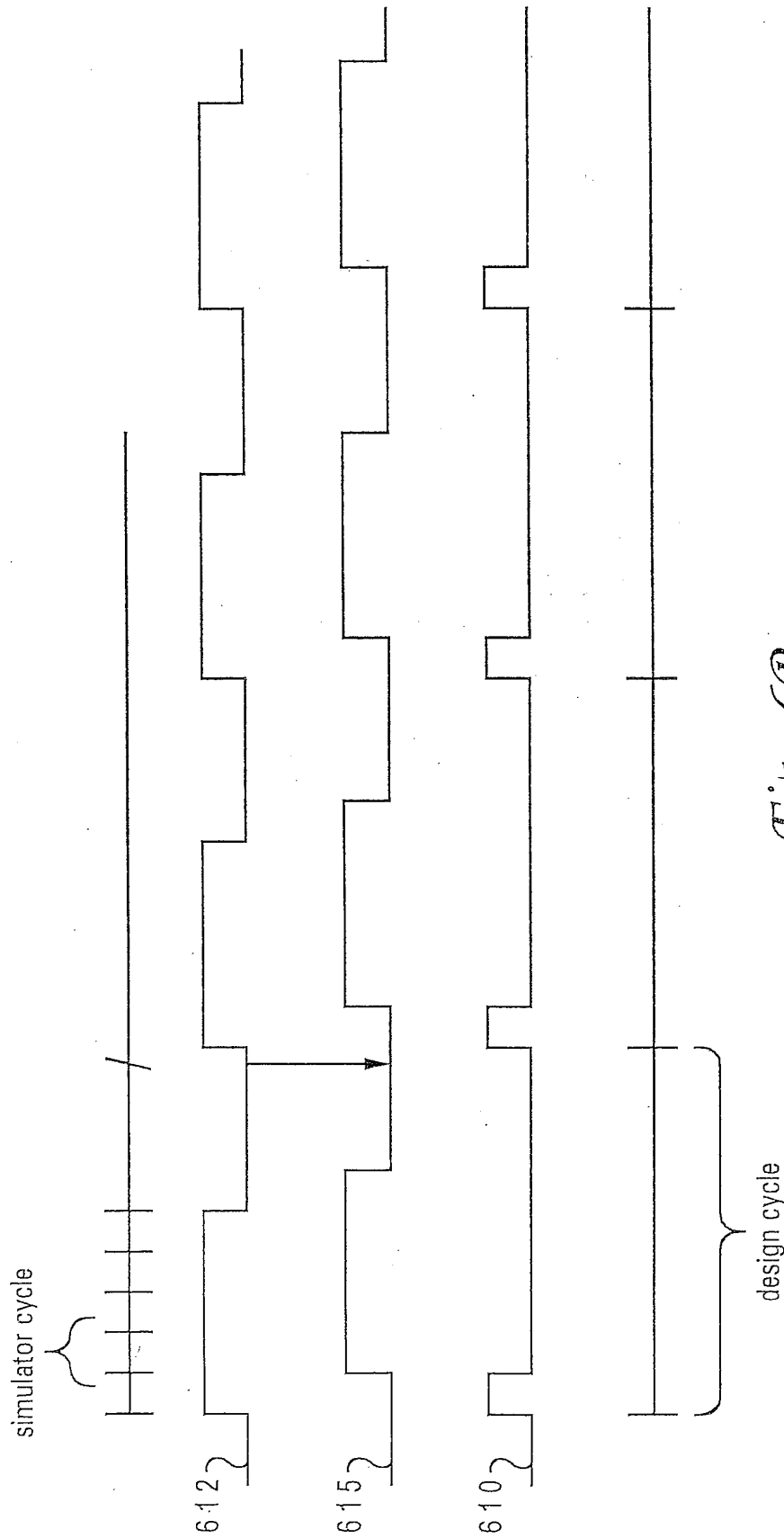


Fig. 6B
(PRIOR ART)

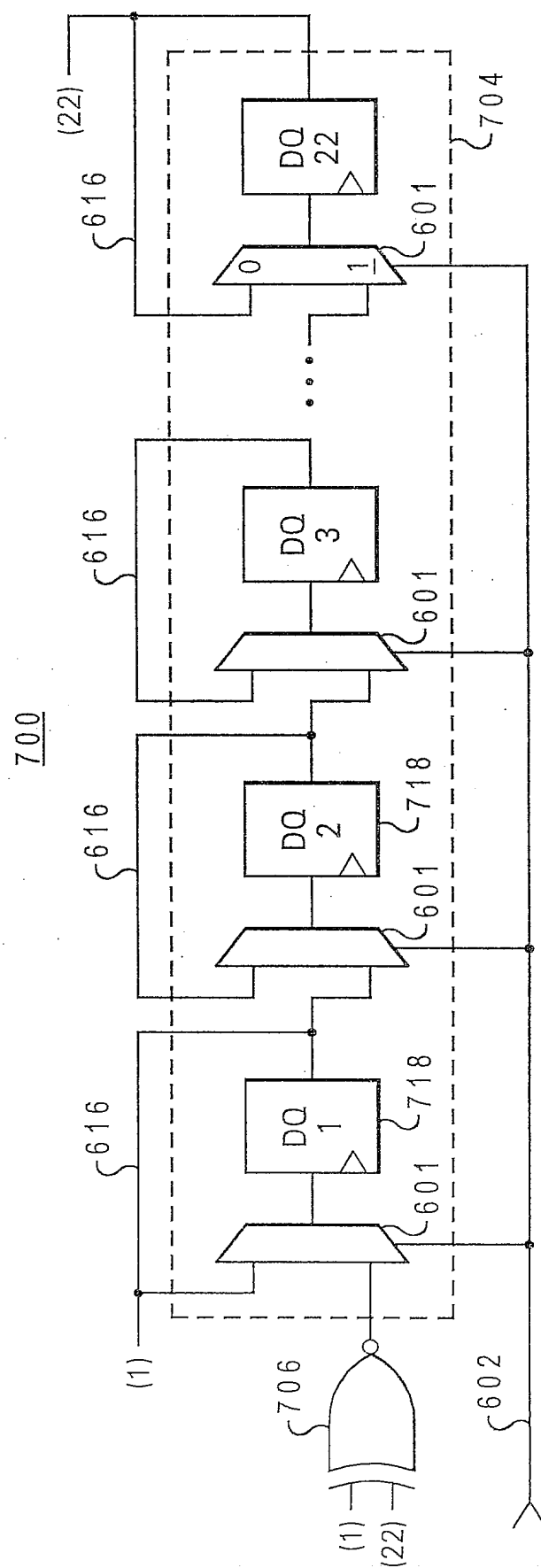


Fig. 7
(PRIOR ART)